Spyridon BLIONAS

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STUDIES

1990 : PhD, (VLSI Design for Parallel Digital Signal Processing), Technical University of Patras (Apr. 86-Jun. 90)
1986 : MSc in Telecommunications, University of Athens
1983 : Diploma in Physics, University of Athens

PROFESSIONAL EXPERIENCE

- Feb. 2021- today : Professor in University of Peloponnese (Electronic Design of Analog and Digital Systems)
- Jul. 2009- today : Associate Professor in University of Peloponnese (Electronic Design of Analog and Digital Systems)
- Feb. 2006- Jul. 2009 : Associate Professor in Technological Educational Institute of Crete (microprocessors, FPGAs)
- Jan. 1999 – Feb. 2006 : Deputy Manager, Emerging Technologies & Markets Dept., INTRACOM S.A., responsible for research activities on design and development of VLSI-ASICs for telecommunication systems, R&D Division, of INTRACOM.
- Oct. 1994 – Dec. 1998 : Microelectronics Section Manager Development Programmes Dept., INTRACOM S.A., responsible for Microelectronics and design and development of VLSI-ASICs for telecommunication systems.
- Dec. 1992 - Sept. 1994 : Research Associate at the Institute of Microelectronics, NCSR Demokritos responsible for design of VLSI-ASICs for digital signal processing.
- Jan. 1991 - Nov. 1992 : Project Coordinator, Development Programmes Dept., INTRACOM S.A., responsible for the VLSI collaborative, research projects on design and development of VLSI-ASICs for telecommunication systems
- Jul. 1989 - Jan. 1991 : Patent Examiner on “Parallel on chip architectures”, European Patent Office (EPO).
- Jan. 1988 - Jun. 1989 : Research fellow at EC Joint Research Center (JRC) Ispra Italy, Electronics Department, on VLSI Design for Telecom Systems.
- Jan. 1985 - Dec. 1987 : Postgraduate scholar at NCSR Demokritos on VLSI Design for Parallel Digital Signal Processing.

- Sep. 1983 -Dec. 1987 Part time prof. (Physics-Electronics in Technical High School).

RESEARCH ACTIVITIES-INTERESTS

- Hardware and software design and development of embedded Internet of Things (IoT) systems, wireless sensor networks.
- Neuroengineering and particularly brain-machine and brain-computer interfaces.
- MEMs and Biosensors
- Analog and Digital Biomedical/Biotechnology systems and Medical devices development
- Methodologies and design of digital signal processing applications
- Reconfigurable architectures

TEACHING EXPERIENCE

- University of Peloponnese, Department of Informatics & Telecommunications Undergraduate Courses:
  - Electronics: 2008-2016 & 2017-2025 (as Lecturer ΠΔ 407/80: 2008-2009)
  - Introduction to Embedded Systems: 2024-Present
  - Internet of Things (IoT): 2022-Present
  - Implementation of Digital Systems and Circuits on FPGAs: 2014-2016 & 2017-2021
  - Design of Digital Circuits and Systems: 2015-2016 & 2017-2019
  - Logic Design: 2011-2013
  - Linear Electrical Circuits: 2009-2013
  - Electronic Telecommunication Systems: 2010-2012
  - Mathematics II: 2014-2015
- Postgraduate Studies Programme (Master's) in Computer Science and Technology:
  - Wireless Sensor Networks: 2013-2016 & 2017-2023
- TEI of Crete, Department of Applied Informatics and Multimedia, School of Technological Applications Undergraduate Courses:
  - Microcomputers: Compulsory Elective Course, 3rd year, 2006-2009
  - Implementation of Digital Wireless Communication Systems in VLSI: Compulsory Elective Course, 3rd year, 2006-2009
  - Embedded Systems: Compulsory Elective Course, 3rd year, 2006-2009
- A.S.E.T.E.M.-SELETE, Department of Electronics
  - Microcomputers: Compulsory Course, 3rd year, 1999-2000

Undergraduate Dissertations (Supervisor or Co-supervisor)

- Stratakos E. (2020)
- Vourkos E. (2020)
- Vottas D. (2020)
- Tsaousis D. (2020)
- Filinis D. (2020)
- Doukas G., Doukas K. (2019)
- Gkikopoulos E. (2019)
- Barkas D. (2018)
- Parapanos A. (2015)
- Christofi Ch. (2015)
- Zarafetas E. (2014)

- Batzoianni E. (2013)

Master's Theses / Diploma Works (Supervisor or Co-supervisor)

- Vezonarakis D. (2025) (MSc in "Computer Science and Technology")
- Manelis G. (2023) (MSc in "Computer Science and Technology")
- Bozis E. Z. (2021) (MSc in "Modern Wireless Communications")
- Zabati A. (2020) (MSc in "Computer Science and Technology")
- Xydis P. (2019) (MSc in "Computer Science and Technology")
- Gasios M. (2010) (MSc in "Advanced Telecommunication Systems and Networks")
- P. Margaronis, (2006) MSc Brunel University
- S. Perdikouris, (2006) MSc Brunel University
- H. Zarakovitis, (2006) MSc Brunel University

Doctoral Dissertations

- Anyfantis A. (2021) (Supervisor)
- Petropoulou A. (2020) (Committee Member)
- I. Ramfos (2015) (University of Patras, Committee Member)
- Poulis S. (Committee Member)

EVALUATOR & REVIEWER OF RESEARCH AND DEVELOPMENT PROJECTS

- General Secretariat for Research & Technology, Greece:
    - Programmes: SYNERGASIA (Cooperation), DIMIOURGO-KAINOTOMO (Create-Innovate), PENNED, YPER.
- European Commission:
    - Programmes/Initiatives: ICT, ESPRIT, OMI.

REVIEWER OF TECHNICAL ARTICLES & CONFERENCE COMMITTEES

Chemosensors Journal, IEEE Internet of Things Journal, Sensors and Actuators Journal, IEICE Information and Communication Technology Forum, Microelectronics Journal, IET Computer & Digital Techniques Journal, Eurosensors Conference, EURO-DAC Conference, EURO-VHDL Conference, Rapid System Prototyping Workshop (Program Committee), IEEE WISES2010 (Program Committee), ICECS 2010, Applied and non-Linear Dynamics from semiconductors to information technologies (member of the organizing committee).

RESEARCH AND DEVELOPMENT PROJECTS

1. 2019-21, "RESEARCH-CREATE-INNOVATE" Programme, Smart Sensor System for Leak Detection in Petroleum Product Pipelines in Noisy Environments (ESTHISIS). Participated in the system's implementation and testing.
2. 2015-2018, FP7-SECURITY-607522, INACHUS, “Technological and Methodological Solutions for Integrated Wide Area Situation Awareness and Survivor Localisation to Support Search and Rescue Teams” leading the design and development of an e-nose system with gas sensors for victim localization in rubble.
3. 2012-2015, «THALES - University of Peloponnese –PROTOMI : Adaptive Technology in Optical Communications».

4. 2009-2013, Corallia Microelectronics cluster “Lab-On-Chip Microelectronic components for Lab-On-Chip Instruments for Genetic Molecular Diagnostics and Environmental Applications”.
5. 2008-2012, IST-216031, CD-Medics, “Coeliac Disease – Management, Monitoring and Diagnosis using Biosensors and an Integrated Chip System”.
6. 2006-2009 IST-027333-ST, Micro2DNA, “Integrated polymer-based micro fluidic micro system for DNA extraction, amplification, and silicon-based detection”
7. 2002-2005, PEPER MILI-A, Wireless mile “SoC for Wireless subscribers connections in Access Network for Advanced Services, GSRT, INTRACOM S.A.
8. 2002-2004 IST-2001-34379, AMDREL “Architectures and Methodologies for Dynamic Reconfigurable Logic”.
9. 2001-2004 IST EASY “Energy aware system-on-chip design of the HIPERLAN/2 project”.
10. 2001-2004 IST ADRIATIC "Advanced Methodology for Reconfigurable SoC and Application Targeted IP-entities in wireless Communications”.
11. 2000-2002 IST SYDIC “System Design Industry Council of European Telecom Industries”.
12. 1999-2000 ESPRIT OCMP TCS_24.123 "One-Chip Low Power Transceiver for Multi-Mode Portable Phones"
13. 1997 ESPRIT LPGD ESD_LP 25.256 "Low-Power Methodology/Flow and its application to the Implementation of a DCS1800-GSM/DECT Modulator - Demodulator”
14. 1997 ESPRIT CODAC OMI_24.129 "Co-design for Applications with Embedded Cores"
15. 1996-99 ESPRIT ASPIS OMI_20.287 "Application Specific Processor and Instruction Set"
16. 1996-1998 FUSE, “First Users Action” Transfer Technology Node (TTN), EC.
17. 1995-97 EPET II 487 "Microelectronics Industrial Projects"
18. 1993 ESPRIT 6043 QUICKCHIPS "A System Supporting ASIC Design and Providing Rapid Turnaround Prototyping".
19. 1992-94 STRIDE HELLAS 187 "Special Action VLSI-ASICs"
20. 1991-92 ESPRIT 5692 " Special Action VLSI-ASICs"
21. 1989-90 ESPRIT 802 "CAD for VLSI Systems, (CVS)", TALTEL.

PARTICIPATION IN PREPARATION OF RESEARCH AND DEVELOPMENT PROPOSALS

As Scientific Coordinator of the proposal:

1. PEL83, 2020, "Advanced platform for agro-cultivation monitoring with disease diagnostic capabilities for precision agriculture, based on self-powered low-consumption sensors, aerial/ground autonomous vehicles, and machine learning techniques (AGRI-BIRDS)."

As Proposal Coordinator and/or Project Coordinator:

2. ELIDEK, 2019, Phase B, "Development of a smart electronic nose (e-nose) rapid prototyping platform, and of Laboratory Infrastructure, for Verification (High Accuracy) of Gas and Volatile Compounds Detection Systems (e-nose)".
3. ELIDEK, 2018, Phase A, "Development of a platform for the rapid prototyping of Smart Electronic Noses (e-nose), and Laboratory Infrastructure for Verification (High Accuracy) of Gas and Volatile Organic Compound Detection Devices (e-nose)."

4. ELIDEK 2018 Phase A, "Integrated Real-Time Localization System for Extreme Sports Participants (REALTRAX)."
5. H2020-SC1-2018, "Personal Persistent Management System for Parkinson's Disease (PERSIST)".
6. H2020-SC1-2018, "Metabolic Diseases Omics Platform (MDomics)".
7. H2020-SC1-2018, "Closed-Loop integrated System for cardiac patients featuring implantable and On-body sensors for monitoring and Regulated drug delivery (COR4LIFE)".
8. Horizon 2020, NMBP 2017, "Point of care microfluidic-based platform for personalized treatment design and monitoring. Case study: osteosarcoma (MICROperOS)".
9. H2020 ICT 2017, "Optofluidic-based Point-of-Care microsystem for therapy prediction in rheumatoid arthritis (OPTIMA)".
10. H2020 ICT 2017, "Photonic biosensor system for decentralised non-invasive Alzheimer's disease screening using mobile communication technologies (televant)".
11. H2020-SC1-2016-RTD, "Lab-on-Chip based On-site detection and remote spread monitoring platform for securing the food chains against multiple animal diseases and biological contaminations (LoC-BioProtect)".
12. H2020-SC1-2016-RTD, "Lab-on-Chip Platform for Fast Pathogen Identification and Accurate Treatment of Infectious Diseases (LoCGen)".
13. H2020-SC1-2016-RTD, "Early toxin alert using an integrated microsystem for the simultaneous detection of multiple seafood toxins (uTOXALERT)".
14. H2020-SC1-2016-RTD, "Cost-effective multi-pathogen detection for rational antibiotic use and detection of resistance in humans and animals (MULTIPATH)".
15. H2020, PHC-2015, "Implantable system for monitoring and stimulating peripheral nerve regeneration (i-Nerve)".
16. H2020, ICT-2015, "Integrated LoC Platform to Track Gene Mutations by Analysing Foetal Cells isolated in Maternal Blood Circulation (FETALFISH)".
17. H2020, ICT-2015, "Fully Automatic Bio-molecular LAB on Chip for multi-target nucleic acid detection (FABLab)".
18. H2020-NMP-29-2015, "High level Integrated SEnsor for NanoToxicity Screening (HISENTS)".
19. FP7-ICT-2013 "Integrated microsystem for fishing and genetic characterisation of foetal cells in maternal blood for screening of haemoglobinopathies (GeneTRACK)".
20. FP7-ICT-2013 "An advanced Lab-on-chip microsystem for theranostics and high safety personalized HEALTH care (microHEALTH)".
21. FP7-ICT-2013 "Integrated Adaptive Support for Chronically Ill by means of Dynamic Therapy PlanS (IASIS)".
22. FP7-ICT-2013, "Closed-Loop System for cARdiac patients featuring intelligent control and Dosimetry (CARDO)".
23. FP7-HEALTH-2012, "Rapid Diagnostic tests for Infectious diseases based on a Lab-on-Chip Platform (DIAGLoC)".
24. FP7-HEALTH-2012, "Intelligent Personal Health System based on the Analysis of Multi-Parametric Data for the Monitoring and Management of Gastroesophageal Reflux Disease Patients (myGERD)".
25. FP7-HEALTH-2011, "Cost-effective multi-analyte detection of pathogens for rational antibiotic use (MULTIPATH)".
26. FP7-HEALTH-2010, "Multi-analyte Lab-on-Chip Platform for Fast Identification of a wide-range of Pathogens and Drug Resistance (LoCRESIST)".

As Work Package Leader:

27. Horizon 2020, NMBP 2017, "A low cost point of care inflammation monitoring kit (inFLAME)".
28. "RESEARCH-CREATE-INNOVATE" 2017, "Development of New Systems for the Detection of Biomolecules, Metabolites and/or other Organic Molecules using Molecularly Imprinted Polymers (BIOMAP)."
29. H2020-SC1-2016-RTD, "Quantum synergy based integrated microsystem for the management of VENTiltor-Associated Pneumonia (Q-VENT)".
30. H2020-LEIT-2015, "Microbial Determination at ISS (BIODETISS)".
31. H2020-PHC-2014 "mobile Smartphone self moniTOring and testing for Personalised smOking cessation (mSTOP)".
32. FP7-ICT-2013, "A Novel, Flexible and Efficient Architecture for Networking and Biology Applications (NEFERTITI)".
33. FP7-HEALTH-2012, "Automated, microfluidic platform for the screening of genetic mutations and diagnosis of cardiomyopathy (CardioGeneScreen)".
34. FP7-HEALTH-2012, "Low-cost screen-printed microsystems for the detection of latent and active neglected infectious diseases in various clinical/field settings (DETECTNEGLECT)".
35. FP7-HEALTH-2011, "Phenotype-Genotype Correlaction Platform Based on High-Throughput Extendible Lab-On-Chip Technology and a Standardized Analysis Platform (GenHELP)".
36. FP7-HEALTH-2011, "Automated, microfluidic platform for genomic analysis and genotyping for high-throughput screening of cardiomyopathies (Cardiomics)".
37. NMP 2011, "Next-GEneration Nano-Imprint lithOgraphy platform for mass manufactUring of multiparameter nano-Sensors (NGENIOUS)".
38. FP7-HEALTH-2010, "Smart Integrated Biodiagnostic Systems for Healthcare (SmartHealth)".
39. FP7-HEALTH-2010, "Continuous Fast airborne Pathogen Monitoring by bio/nano-to-macro interfacing (FastPath)".
40. FP7-HEALTH-2010, "Multi-faceted μTAS for the screening of sputum samples and blood samples on lung cancer based on the isolation of circulating tumor cells and free DNA (LUCATAS)".

ADMINISTRATIVE WORK

- **University of Peloponnese**
  - *Department of Informatics and Telecommunications*
    - Head of Department: Sep. 2020 - Aug. 2021
    - Vice Head of Department: 2013-2020
    - Director of the Inter-institutional Postgraduate Studies Programme (P.M.S.) "Space Science, Technologies and Applications": 2017-2018, 2019-2025
    - Director of the Electronics Laboratory: 2023-Present
    - Director of the Computational Systems Laboratory: 2018-2023
    - Deputy Director of the Inter-institutional Postgraduate Studies Programme (P.M.S.) "Space Science, Technologies and Applications": 2018-2019
    - Member of the Special Inter-institutional Committee for the M.Sc. "Space Science, Technologies and Applications": 2017
    - Member of the Internal Evaluation Team (OmEA): 2014-Present
    - Deputy Representative of the Department in the Research Committee of the Special Account for Research Funds (ELKE): 2015

- Representative of the Department in the Research Committee of the Special Account for Research Funds (ELKE): 2016-2017
- Member of various committees (Teaching Experience, EDIP Transfers, Good Performance), 2009-Present

- *School of Economics and Technology*
  - Member of the Faculty Assembly (Deanery Assembly): 2013-2022
- *University of Peloponnese (Central Level)*
  - Member of the Senate: Sep. 2020 - Aug. 2021
  - Alternate Member of the Senate: 2013-2020

- **INTRACOM S.A.**
  - *General Directorate of Research & Development*
    - Deputy Director of Development Programs, Responsible for research activities in the design and implementation of telecommunication systems using Application-Specific Integrated Circuits (VLSI-ASICs): 1999 – 2006
  - *Development Programs Department*
    - Responsible for Microelectronics research activities and the design of Application-Specific Integrated Circuits (VLSI-ASICs) for Telecommunication Systems, General Directorate of Research & Development: 1994-1998

- **Scientific Coordinator of nine research projects:**
  - FP7-SECURITY-607522 (INACHUS)
  - IST-027333-ST (Micro2DNA)
  - ESPRIT OCMP TCS_24.123
  - ESPRIT LPGD ESD_LP 25.256
  - ESPRIT CODAC OMI_24.129
  - ESPRIT ASPIS OMI_20.287
  - EPET II 487
  - STRIDE HELLAS 187
  - ESPRIT 5692

PhD Thesis

Spyridon Blionas: "Design of Very Large Scale Integration Circuits for Parallel Digital Signal Processing" University of Patras, Department of Electrical and Computer Engineering, Integrated Circuits Design Laboratory.

JOURNAL PUBLICATIONS

J1. Anyfantis A, Blionas S. “An Analysis on the Performance of a Mobile Platform with Gas Sensors for Real Time Victim Localization”, Sensors, 2021; 21(6):2018. https://doi.org/10.3390/s21062018

J2. S. Blionas, “Wind and Temperature Effect on the Performance of a Mobile e-nose platform for Real Time Victim Localization”, 2021 J. Phys.: Conf. Ser. 1730 012121.

J3. S. Blionas, “Expected Performance of a Mobile e-nose platform for Real Time Victim Localization”, 2021 J. Phys.: Conf. Ser. 1730 012120.

J4. A. Anyfantis, S. Blionas, “Proof of concept apparatus for the design of a simple, low cost, mobile e-nose for real-time victim localization (human presence) based on indoor air quality monitoring sensors”, Sensing and Bio-Sensing Research, Volume 27, February 2020, 10031.

J5. I. Ramfos, S. Blionas and A. Birbas, “Architecture of a modular, multichannel readout system for dense electrochemical biosensor microarrays”, IOP Publishing, Measurement Science and Technology, Vol. 26, No 1, (24 November 2014)

J6. I. Ramfos, N. Vassiliadis, S. Blionas, K. Efstathiou, A. Fragoso, C. K. O'Sullivan, “A compact hybrid-multiplexed potentiostat for real-time electrochemical biosensing applications” Elsevier, Biosensors and Bioelectronics, Vol. 47 (15 September 2013), p.p. 482–489

J7. G. Kornaros, A. Demiris, S. Blionas : "Lab-on-Chip for Pharmacogenomics: An Embedded System Organization", Micro and Nanosystems Bentham Science Publishers, Volume 1, No1, 2009

J8. G. Kornaros, S. Blionas : "Microarchitecture of a Lab-on-Chip Microarray for Pharmacogenomics and Molecular Diagnostics," EURASIP Journal on Advanced Signal Processing, Volume 2008, Article ID 520641, 11 pages, doi:10.1155/2008/520641.

J9. Labros Bisdounis, Spyros Blionas, Enrico Macii, Spiridon Nikolaidis, and Roberto Zafalon "Implementation Strategy and Results of an Energy-Aware System-on-Chip for 5 GHz WLAN Applications", Journal of Low-Power Electronics, American Scientific Publishers, vol. 2, no. 1, April 2006.

J10. S. Nikolaidis, N. Kavvadias, T. Laopoulos, L. Bisdounis, S. Blionas, “Instruction Level Energy Modeling for Pipelined Processors”, Journal of Embedded Computing 1, IOS Press, Mar. 2005, p.p.317–324.

J11. A. Pnevmatikakis, S. Blionas and D. Triantis, “Physical Layer of Base-Band OFDM Modem - Algorithms and Performance”, J. Circuits, Systems and Computers, vol. 14, no.3, June 2005

J12. C. Drosos, D. Metafas, S. Blionas and G. Papadopoulos, “Rapid prototyping of a wireless LAN implementation using a UML-based system design methodology”, IEICE Trans. on Information and Systems, Trans. on Information and Systems, Vol.E87-D, No.8, August, 2004, p.p. 2058-2069.

J13. C. Drosos, C. Dre, D. Metafas, D. Soudris, S. Blionas, “The Low Power Analogue and Digital Baseband Processing Parts of a Novel Dual Mode DECT/DCS1800 Terminal”, Microelectronics Journal, ELSEVIER Vol 35, No. 7, July 2004, pp 609-620.

J14. C. Drosos, L. Bisdounis, D. Metafas, S. Blionas, A. Tatsaki, G. Papadopoulos, "Hardware-software design and validation framework for wireless LAN modems", IEE Proceedings Computers and Digital Techniques, vol. 151, no. 3, pp. 173-182, May 2004.

J15. L. Bisdounis , C. Dre , S. Blionas , D. Metafas , A. Tatsaki , F. Ieromnimon , E. Macii , Ph. Rouzet , R. Zafalon , L. Benini, “A Low-Power System-on-Chip (SoC) Architecture for Wireless LANs”, IEE Proceedings – Computers & Digital Techniques, Vol. 151, No. 1, January 2004, p.p. 2-15

J16. K. Tatas, K. Siozios, D. Soudris, K. Masselos, K. Potamianos, S. Blionas and A. Thanailakis, “Power Optimization Methodology for Multimedia Applications Implementation on Reconfigurable Platforms”, LNCS series, (Lecture Notes in Computer Science, Springer Verlag), Field Programmable Logic and Applications, vol. 2799, pp.430-439, 2003

J17. K. Masselos1, A. Pelkonen2, M. Cupak, S. Blionas, “Realization of Wireless Multimedia Communication Systems on Reconfigurable Platforms”, invited paper, Journal of Systems Architecture, Special Issue on Reconfigurable Systems, (Elsevier), Volume 49, Issues 4-6 , September 2003 , p.p. 155-175

J18. C. Drosos, C. Dre, S. Blionas, and D. Soudris, "A low power baseband processor for a portable dual mode DECT/GSM terminal", IEICE Trans. on Information and Systems, Vol.E86-D, No.10, October, 2003, p.p. 1976-1986

J19. S. Blionas et al., "Prototyping of a 5 GHz WLAN Reconfigurable System-on-Chip", IEICE Trans. on Information and Systems, Vol. E86-D, No. 5 May 2003, p.p. 891-900.

J20. G. Koutroumpezis, K. Tatas, D. Soudris, S. Blionas, K. Masselos, and A. Thanailakis, "Architecture Design of a Reconfigurable Multiplier for Flexible Coarse-grain Implementations LNCS series, (Lecture Notes in Computer Science, Springer Verlag), Field Programmable Logic and Applications, vol. 2438, pp.1080-1083, September 2002.

J21. S. Blionas, et al., "A HIPERLAN/2-IEEE 802.11a Reconfigurable System-on-Chip", LNCS series, (Lecture Notes in Computer Science, Springer Verlag), Field Programmable Logic and Applications, vol. 2438, pp. 1027-1036, September 2002.

J22. H. Karathanasis, C. Dre, D. Metafas and S. V. Blionas, "Designing a Single chip DSP for DECT and GSM/DCS-1800 Baseband Processing", Real Time Magazine, September 1996, p22-31.

J23. H. C. Karathanasis, C. N. Dre, D. E. Metafas and S.V. Blionas, "On the Design of a Baseband Processor for DECT and GSM/DCS-1800", Embedded Microprocessor Systems, C. Muller-Schloer et al. (Eds.), IOS Press, 1996, ISBN 90 5199 300 5 (IOS Press), ISDN 4 274 90122 X C3054 (Ohmsha).

J24. Stavrakakis G.N., Blionas S.V., and Goutis C.E., "Dynamic Source Parameters of Corinth (central Greece) Earthquake sequence based on FFT and Iterative Maximum Entropy Techniques", Tectonophysics, Vol. 185, pp. 261-275, 1991.

J25. Stavrakakis G.N., Blionas S.V., "Source Parameters of Some Large Earthquakes in the Eastern Mediterranean Region Based on an Iterative Maximum Entropy Technique", Pure appl. Geophys., (PAGEOPH), Vol. 132 No. 4 pp. 679-698, 1990.

CONFERENCES PUBLICATIONS

C1. A. Anyfantis, S. Blionas, "Design and Development of a Mobile e-nose platform for Real Time Victim Localization in Confined Spaces During USaR Operations", IEEE International Instrumentation and Measurement Technology Conference (I2MTC 2020), 25–28 May 2020, Valamar Lacroma, Dubrovnik, Croatia.

C2. S Blionas, G Doukas, K Doukas, N. D. Tselikas, "A Flexible/Scalable IoT Server Node testbed, from Gateway to Edge Computing. A Smart Home Use Case", Panhellenic Conference on Electronics & Telecommunications (PACET 2019), 8–9 November 2019, Volos, Greece.

C3. A Anyfantis, S Blionas, "Indoor air quality monitoring sensors for the design of a simple, low cost, mobile e-nose for real time victim localization", Panhellenic Conference on Electronics & Telecommunications (PACET 2019), 8–9 November 2019, Volos, Greece.

C4. I. Stamoulias, K. Georgoulakis, S. Blionas and G.O. Glentis, FPGA "Implementation of an MLSE Equalizer in 10Gb/s Optical Links", 2015 IEEE International Conference on Digital Signal Processing (DSP), Singapore, 21-24 July 2015.

C5. J. Stamoulias, S. Blionas, "Systolic Architecture of a Viterbi Equalizer for Optical Communications", 2015 4th Workshop on Modern Circuit and Systems Technologies, University of Thessaloniki, 14-15 May 2015.

C6. S. Blionas, G. Papadourakis, "Implementation performance of an Embedded Architecture for Lab-on-Chip Instrumentation Control and Data Analysis", AmiEs-2013 – 12th International Symposium on Ambient Intelligence and Embedded Systems, 19–22 September 2013, Berlin, Germany.

C7. S. Blionas, "An Embedded Architecture for Lab-on-Chip Instrumentation Control and Data Analysis", AmiEs-2012 – 11th International Symposium on Ambient Intelligence and Embedded Systems, 20th – 22nd September 2012, Espoo, Finland.

C8. C.-L. Sotiropoulou, L. Voudouris, C. Gentsos; S. Nikolaidis, N. Vassiliadis, A. Demiris, S. Blionas, "FPGA-based machine vision implementation for Lab-on-Chip flow detection", Symposium on Circuits and Systems (ISCAS), 2012 IEEE International, 20-23 May 2012.

C9. S. Blionas, "Design methodology for implementation of the physical layer of multi-standard Reconfigurable Systems-on-Chip (RSoCs) for Wireless Communications", 2012 Workshop on Modern Circuit and Systems Technologies, University of Thessaloniki, 16 March 2012.

C10. S. Blionas, "Scalable low cost Architecture for Analysis of Lab-on-Chip Data", 17th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2010, December 2010.

C11. S. Blionas, "Digital and Analogue Components for a System, for Lab-on-a-Chip", invited talk, WISES 2010, 8th IEEE Workshop on Intelligent Solutions in Embedded Systems, Heraklion, Crete, Greece, 8-9 July 2010.

C12. S. Blionas, "A system for Molecular Diagnostics", 4th Concertation and Consultation Workshop on Micro-Nano-Bio Convergence Systems MNBS 2010, CSEM Neuchâtel, Switzerland, 15-16 February 2010.

C13. S. Blionas, A. Demiris, Latest Developments in Integrated polymer-based micro-fluidic micro-system for DNA extraction, amplification, and silicon-based detection", invited talk, Third International Workshop on Multianalyte Biosensing Devices, Athens, Greece, 18-19 September 2008.

C14. G. Kornaros, D. Meidanis, S. Chatzandroulis, Y. Papaefstathiou, and S. Blionas: "Architecture of a Consumer Lab-On-Chip for Pharmacogenomics", IEEE Conference on Consumer Electronics, Las Vegas, published January 2008.

C15. S. Blionas, "Integrated polymer-based micro-fluidic micro-system for DNA extraction", invited talk, 4th International Conference on Personalised Health, Chalkidiki, Greece, 20-22 June 2007.

C16. S. Bellis, S. Blionas, J. Carrera, S. Chatzandroulis, P. Galvin, S. Getin, M. Gheorghe, K. Misiakos, A. Planat-Chretien, J. Ragoussis, and D. Tsoukalas, "Alternatives for an integrated microfluidic Microsystem incorporating, DNA extraction, DNA amplification and Electronic Hybridisation Detection for diagnosis genetic tests applications", Discovery2Diagnostics Conference, Boston, MA, USA, 25-27 September 2006.

C17. S. Bellis, S. Blionas, J. Carrera, S. Chatzandroulis, S. Getin, K. Misiakos, A. Planat-Chretien, D. Tsoukalas, "Competitive technology approaches for Electronic Hybridisation Detection in a microsystem with microfluidics for diagnosis genetic tests", Proceedings of 28th IEEE EMBC Annual International Conference, New York City, USA, Aug 30-Sept 3, 2006, pp. 4103-06.

C18. M. Gheorghe, S. Blionas, J. Ragoussis, and P. Galvin, "Evaluation of Silicon and Polymer substrates for fabrication of integrated microfluidic microsystems for DNA extraction and amplification", Proceedings of 28th IEEE EMBC Annual

International Conference, New York City, USA, Aug 30-Sept 3, 2006, pp. 2485-88.

C19. Panagiotis Margaronis, Spyros Blionas, Emmanouel Antonidakis, Markos Kimionis, Marios Hadjinikolaou, "Design and implementation of Automatic Gain Control (AGC) and Radio Signal Strength (RSSI), circuitry for an OFDM reconfigurable transceiver", Proceedings of the Annual Conference on Telecommunications & Multimedia-TEMU 2005, 23-26 June 2005, Heraklion, Crete, pp. 361-368.

C20. S. Perdikouris, M. Hadjinikolaou, S. Blionas, E.Antonidakis, "Firmware design approach for an Access Point embedded system of a Hiperlan/2 WLAN", Proceedings of the Annual Conference on Telecommunications & Multimedia-TEMU 2005, 23-26 June 2005, Heraklion, Crete, pp. 388-394.

C21. H. Zarakovitis, S. Blionas, E. Antonidakis, M. Hadjinikolaou, "Firmware design approach for a Mobile Terminal embedded system of a Hiperlan2 Wireless Local Area Network", Proceedings of the Annual Conference on Telecommunications & Multimedia-TEMU 2005, 23-26 June 2005, Heraklion, Crete, pp. 395-403.

C22. Labros Bisdounis, Spyros Blionas, Enrico Macii, Spiridon Nikolaidis, and Roberto Zafalon, "Energy-Aware System-on-Chip for 5 GHz Wireless LANs", Int. Workshop on Power and Timing Modeling, Optimization and Simulation, Santorini, Greece, Sep. 2005.

C23. C. Drosos, L. Bisdounis, D. Metafas, S. Blionas, A. Tatsaki, "A Multi-level Hardware-Software Validation Methodology for Wireless Network Applications ",Int. Workshop on Power and Timing Modeling, Optimization and Simulation, Santorini, Greece, Sep. 2004.

C24. K. Masselos, S. Blionas, J-Y. Mignolet, A. Foster, D. Soudris, S. Nikolaidis, "Hardware Building Blocks of a Mixed Granularity Reconfigurable System-on-Chip Platform", Int. Workshop on Power and Timing Modeling, Optimization and Simulation, Santorini, Greece, Sep. 2004.

C25. Masselos, D. Soudris, S. Blionas, "A Reconfigurable System-on-Chip Platform for Wireless Communications", IEEE Int. Workshop on Wireless Circuits and Systems Vancouver, Canada, May 2004.

C26. E. Theochari 1 , K. Tatas D. J. Soudris, Masselos, K. Potamianos, S. Blionas and A. Thanailakis, "A reusable ip fft core for dsp applications", IEEE International Symposium on Circuits and Systems 2004 (IEEE ISCAS 2004), Vancouver, Canada, May 2004.

C27. S. Nikolaidis, N. Kavvadias, T. Laopoulos, L. Bisdounis, S. Blionas, "Instruction Level Energy Modeling for Pipelined Processors", Int. Workshop on Power and Timing Modeling, Optimization and Simulation, Torino, Italy, Sep. 2003.

C28. D. Soudris, M. Kesoulis, C. Koukourlis, S. Blionas, "Alternative direct digital frequency synthesizer architectures with reduced memory size", IEEE International Symposium on Circuits and Systems 2003 (IEEE ISCAS 2003), Bangkok,Thailand, May 2003.

C29. K. Masselos, S. Blionas, "Reconfigurability requirements of wireless communication systems" IEEE Workshop on Heterogeneous reconfigurable Systems on Chip (SoC), Chances, Applications, Trends, April 2002, Hamburg, Germany.

C30. D. Soudris, K. Masselos, S. Blionas, S. Siskos, S. Nikolaidis and K. Tatas, "AMDREL: On Designing an Embedded FPGA Structure for the Future Reconfigurable SoC for Wireless Communication Applications", IEEE Workshop

on Heterogeneous reconfigurable Systems on Chip (SoC), Chances, Applications, Trends, April 2002, Hamburg, Germany.

C31. S. Blionas, K. Masselos, C. Dre, F. Ieromnimon, T. Pagonis, A. Pneymatikakis, A. Tatsaki, T.Trimis, A. Vontzalidis and D. Metafas, "Design Story : A Hiperlan2/IEEE802.11x Reconfigurable SoC for indoor WLANs and outdoor wireless links. A pilot project for the future generation configurable wireless communications products" IEEE Workshop on Heterogeneous reconfigurable Systems on Chip (SoC), Chances, Applications, Trends, April 2002, Hamburg, Germany.

C32. C. Drosos, C. Dre, D. Metafas, D. Soudris, S. Blionas, "The low power baseband processing parts of a novel dual mode DECT/GSM terminal", International IEEE Conference on Electronics, Circuits, and Systems (ICECS), 2-6 Sept. 2001, Malta.

C33. C.Drosos, C. Dre, S. Blionas, D. Soudris "On the implementation of a baseband processor for a portable Dual Mode DECT/GSM terminal" , IEEE International Symposium on Circuits and Systems, (ISCAS), May 6 - 9, 2001 Sydney, Australia ISCAS'2001, Sydney.

C34. Drosos, C. Dre, K. Potamianos and S. Blionas, "A MCM-L Board for the Basaband Processor of a Dual Mode Wireless Terminal", MMN 2000 (First Conference on Microelectronics, Microsystems and Nanotechnology), 20-22 November 2000.

C35. F. Ieromnimon, C. Dre, D. Metafas, C. Drosos, V. Koratzinos, A. Alexopoulou, S. Blionas, "On the Integration of Diverse Testing Strategies in a Low-Power Processor", Design Automation & Test in Europe Conference (DATE2000), Paris, France, March 2000.

C36. C. Drosos, C. Dre, D. Soudris, G. Kalivas and S. Blionas "On the Design of a Low Power Modulator/Demodulator for DECT/GSM", in Proc. of 1st Conf. Microelectronics, Microsystems, & Nanotechnology, November 20-22, 2000, Athens, pp. 309-312.

C37. H. Karathanasis, C. Dre, D. Metafas and S. Blionas "On Designing a DSP for DECT and GSM/DCS1800 Baseband Processor", EMSYS 96 OMI sixth Annual Conference, Berlin, September 1996.

C38. D. Metafas, H. Karathanasis, and S. Blionas "Industrial Approach in Designing Methodologies for Mobile Communications Systems", Seventh IEEE International Workshop on Rapid System Prototyping, Thessaloniki, Greece, June 1996.

C39. S. Blionas, I. Bogdos, A. Bonomo, M. Italiano, L. Lavagno, M. L. Maggiulli, M. Mesturino, M. Paolini, I. Stamelos, "ASIC Design with the BACH Behavioural Synthesis System" The European Design Automation Conference Glasgow, Scotland Poster Session 2, March 1990.

C40. S. Blionas, A. Balboni, G. Gorla, "A VLSI Linear Array of Processors for the Viterbi Algorithm Designed with an Approach Independent from Design Language and from Implementation Technology" Proc. Int'l Conf. on VLSI and CAD pp. 67-70 Octob. 1989.

C41. S. Blionas A. Balboni, G. Gorla, S. Barbagalo, A. Burri, R. Castellan, S. Ravaglia, "A Special Purpose Technology Independent SIMD Parallel Processor for the Viterbi Algorithm", Proc. of IFIP Workshop on Parallel Architectures on Silicon: from Systolic Arrays to Neural Networks ", Grenoble France pp. 227-239, December 1989.

C42. C.E. Goutis and S.V. Blionas, "Array processor for solving noisy Toeplitz systems", in Proceedings of conference in Integrated Circuit Technology I, Limerick, Ireland, pp. 65-72, 1986.

PATENT APPLICATIONS

- Greek Patent Application : S. Blionas, A. Demiris, GR20130100091, 31 January 2013 ("Integrated System for electronic detection of biological components with Visual Control, based on Microfluidics (Lab-on-Chip)")
- Greek Patent Application : I. Ramfos, S. Blionas, GR20120100269, 22 May 2012, ("Parameterisable, autocallibrated circuit for parallel measurements of electrochemical sensors under continuous bias")
- Greek Patent Application : A. Demiris, S. Blionas, GR20110100390/2011-02211, 5 July 2011 ("Integrated System for the Visual Control, Quantitative and Qualitative Flow Measurement in Microfluidics")
- European Patent Application : S. Blionas, "Viterbi Equaliser for Maximum Likelihood Estimation", EP0671836A2, European Patent Office, *1995*.
- Greek Patent Application : S. Blionas, "Viterbi Equaliser for Maximum Likelihood Estimation", GR 94010109, O.B.I. *1994*.

Technical Reports (Deliverables of R&D projects)

IR1. A. Anyfantis, S. Blionas, "D5.4.4 Development and Testing of the Final Prototype of a Chemical-based identification of human presence in narrow spaces", 31/12/2018.

IR2. Α. Δεμίρης, S. Blionas, A. Anyfantis, "INACHUS Exploitation Plan and Pre-Commercial Procurement Strategy", 30/06/2018.

IR3. A. Anyfantis, S. Blionas, "D5.4.3 Development and Testing of the Second Prototype of a Chemical-based identification of human presence in narrow spaces", 31/12/2017.

IR4. A. Anyfantis, S. Blionas, A. Silis, "D5.4.2 Development and Testing of the First Prototype of a Chemical-based identification of human presence in narrow spaces", 31/12/2016.

IR5. A. Anyfantis, A. Silis, S. Blionas, "D5.4.1 Specifications of a Chemical-based identification of human presence in narrow spaces", 31/12/2015.

IR6. A. Silis, J. Lukasiak, S. Blionas, Α. Δεμίρης, «Π5.1 Υλοποίηση και testing Lab-on-a-chip devices με ενσωματωμένους βιοαισθητήρες και με on-chip electronic DNA hybridization detection και PCR, για διάγνωση μολυσματικών ασθενειών», 31/12/2015.

IR7. Α. Εμερετλής, Ι. Σταμούλιας, Β. Κελεφούρας, S. Blionas, Γ. Θεοδωρίδης, Κ. Γκούτης, «Π4.4.2: Μελέτη της απόδοσης των διαφορετικών αλγορίθμων ηλεκτρονικής προσαρμογής σε οπτική μετάδοση», 30/11/2015.

IR8. Γ. Σταμούλιας, S. Blionas, «Π4.4.1: Τελικό πρωτότυπο του Εξισωτή πιθανοφάνειας οπτικής μετάδοσης Viterbi Radix 2 & Radix 4 Fixed Point, Blocking, Systolic Architecture, Adaptive, Euclidean & Mahalanobis metrics», 30/06/2015.

IR9. Α. Δεμίρης, S. Blionas, A. Anyfantis, A. Silis, «Π4.1 Σχεδιασμός Lab-on-a-chip με ενσωματωμένους βιοαισθητήρες και με on-chip electronic DNA hybridization detection και PCR, για διάγνωση μολυσματικών ασθενειών», 30/04/2015.

IR10. Γ. Σταμούλιας, S. Blionas, «Π4.3: VHDL μοντέλο του Εξισωτή πιθανοφάνειας οπτικής μετάδοσης Viterbi Radix 2 & Radix 4 Fixed Point, Blocking, Systolic Architecture, Adaptive», 31/12/2014.

IR11. S. Blionas, A. Anyfantis, A. Δεμίρης, A. Silis, «Π3.1, Σχεδιασμός Lab-on-a-chip με ενσωματωμένους βιοαισθητήρες και με on-chip electronic DNA hybridization detection για διάγνωση μολυσματικών ασθενειών», 31/12/2014.

IR12. Γ. Σταμούλιας, S. Blionas, «Π4.1.3: Εξισωτής πιθανοφάνειας οπτικής μετάδοσης Viterbi Radix 2 & Radix 4 Fixed Point, Blocking, Systolic Architecture, Adaptive» , 30/06/2014.

IR13. Γ. Σταμούλιας, D. Barkas, S. Blionas, «Π4.2: Βιβλιοθήκη υψηλού επιπέδου (SystemC) του συνολικού συστήματος του Εξισωτή πιθανοφάνειας οπτικής μετάδοσης Viterbi Radix 2 & Radix 4 Fixed Point, Blocking», 31/12/2013.

IR14. A. Anyfantis, A. Δεμίρης, A. Silis, S. Blionas, «Π2.1 Σχεδιασμός Lab-on-a-chip με ενσωματωμένους βιοαισθητήρες για διάγνωση μολυσματικών ασθενειών», 31/12/2013.

IR15. Γ. Σταμούλιας, S. Blionas, «Π4.1.2: Εξισωτής πιθανοφάνειας οπτικής μετάδοσης Viterbi Radix 2 & Radix 4 Fixed Point, Blocking», 30/06/2013.

IR16. Γ. Σταμούλιας, S. Blionas, «Π4.1.1: Εξισωτής πιθανοφάνειας οπτικής μετάδοσης Viterbi Radix 2 & Radix 4 Fixed Point» , 30/04/2013.

IR17. Γ. Γεωργούσης, S. Blionas, I. Ράμφος, N. Βασιλειάδης, Σ. Νικολαΐδης, «Π5.4 Προσαρμογές των υποσυστημάτων για περαιτέρω εφαρμογές σε κλινική διαγνωστική», 31/12/2012.

IR18. N. Βασιλειάδης, Γ. Τσελίκης, S. Blionas, I. Ράμφος, «Π4.5 Σχεδιασμός-Μελέτη ανάπτυξη και testing ανάπτυξη Ολοκληρωμένου πρωτοτύπου Point-of-Care Συστήματος, για Μοριακές Αναλύσεις», 31/10/2012.

IR19. Α. Μωραΐτης, Γ. Τσελίκης, S. Blionas, I. Ράμφος, «Π2.7 Σχεδιασμός-Μελέτη ανάπτυξη και testing υλικολογισμικού για το ενσωματωμένο σύστημα ελέγχου, για Όργανα Μοριακών Αναλύσεων», 30/04/2012.

IR20. Σ. Χατζανδρούλης, N. Βασιλειάδης, S. Blionas, I. Ράμφος, «Π3.3 Σχεδιασμός-Μελέτη ανάπτυξη και testing Αναλογικο-ψηφιακού υποσυστήματος ελέγχου και ανάλυσης βιοαισθητήρων, για Όργανα Μοριακών Αναλύσεων», 30/04/2011.

IR21. Χ. Ανδρουλιδάκης, Η. Λαμπρινός, Κ. Σωτηροπούλου, N. Βασιλειάδης, S. Blionas, «Π2.6 Σχεδιασμός-Μελέτη ανάπτυξη και testing ψηφιακού υποσυστήματος μηχανικής όρασης και συμπίεσης εικόνας, για Όργανα Μοριακών Αναλύσεων», 31/10/2011.

IR22. A. Anyfantis, S. Blionas, Ioannis Ramfos, "D6.4 System Validation of a Point of Care System using Biosensors and Integrated Lab on a Chip for Coeliac Disease Management Monitoring and Diagnosis", 31/07/2011.

IR23. Σ. Νικολαΐδης, N. Βασιλειάδης, S. Blionas, I. Ράμφος, «Π2.5 Μεθοδολογία testing υποσυστημάτων ελέγχου και μηχανικής όρασης, για Όργανα Μοριακών Αναλύσεων», 30/04/2011.

IR24. Ioannis Ramfos, A. Anyfantis, A. Demiris, S. Blionas, "D6.3 Verification report of a Point of Care System using Biosensors and Integrated Lab on a Chip for Coeliac Disease Management Monitoring and Diagnosis", 31/01/2011.

IR25. N. Βασιλειάδης, S. Blionas, A. Δεμίρης, «Π2.4 Αλγόριθμοι ανάλυσης εικόνας και μηχανικής όρασης για το αντίστοιχο υποσύστημα, για Όργανα Μοριακών Αναλύσεων», 31/10/2010.

IR26. Σ. Νικολαΐδης, S. Blionas, I. Ράμφος, N. Βασιλειάδης, «Π2.2 Τεχνικές προδιαγραφές Αναλογικο-ψηφιακού υποσυστήματος ελέγχου και ανάλυσης βιοαισθητήρων, για Όργανα Μοριακών Αναλύσεων», 31/10/2010.

IR27. Σ. Χατζανδρούλης, N. Βασιλειάδης, S. Blionas, I. Ράμφος, «Π1.1 Τεχνικές προδιαγραφές βιοαισθητήρων, για Όργανα Μοριακών Αναλύσεων», 31/10/2010.

IR28. Ν. Βασιλειάδης, S. Blionas, Ι. Ράμφος, «Π2.1 Αρχικές δοκιμές και μετρήσεις των συστημάτων πειραματικών μικρορροϊκών διατάξεων, για Όργανα Μοριακών Αναλύσεων», 30/04/2010.

IR29. Ioannis Ramfos, A. Anyfantis, A. Demiris, S. Blionas, "D6.2 Integration and Prototyping of a Point of Care System using Biosensors and Integrated Lab on a Chip for Coeliac Disease Management Monitoring and Diagnosis", 31/01/2010,

IR30. I. Lamprinos, A. Demiris, S. Blionas, "D5.3 Verification of PoC and EMR communication", 31/01/2010.

IR31. Richard Klemm, Claudia Gärtner, S. Blionas. A. Anyfantis, "D4.2 Realisation and validation of individual functional modules", 31/07/2009.

IR32. Xenia Strobach, A. Anyfantis, A. Demiris, S. Blionas, "D1.2 Detailed Specifications report of a Point of Care System using Biosensors and Integrated Lab on a Chip for Coeliac Disease Management Monitoring and Diagnosis" 31/07/2009.

IR33. I. Lamprinos, A. Demiris, S. Blionas, "D5.2 PoC and EMR communication development report", 30/04/2009

IR34. Richard Klemm, Claudia Gärtner, S. Blionas. A. Demiris, A. Anyfantis, "D4.1 Design concept of integrated microfluidic device & functional modules", 31/01/2009.

IR35. A. Anyfantis, S. Blionas, "D6.1 Preliminary Specifications report of a Point of Care System using Biosensors and Integrated Lab on a Chip for Coeliac Disease Management Monitoring and Diagnosis", 31/07/2008

IR36. S. Blionas, A. Demiris, "D 3.4 Data Manager User Manual (assay development, assay progress monitoring, auto-calibration, data storage and transfer, data analysis and presentation, PoC firmware upgrade)", Micro2DNA project, 31/01/2008

IR37. S. Blionas, J. Carrera, "D 7.2 A technology survey reporting the state of the art in the area of DNA biochip testing and SNP detection and identifying Micro2DNA competitor and complementary technologies", Micro2DNA project, 28/02/2008

IR38. J. Carrera, S. Blionas, "D 7.1 A market analysis summarizing opportunities, strengths, weakness and threats for the development of a commercial Point of Care SNP detection system based on Micro2DNA technology", Micro2DNA project, 31/12/2007

IR39. S. Blionas, A. Demiris, "D 3.3 Data Manager Verification Plan & Reports (assay development, assay progress monitoring, auto-calibration, data storage and transfer, data analysis and presentation, PoC firmware upgrade)", Micro2DNA project, 30/11/2007

IR40. S. Blionas, "D 4.2 Instrument Design Report (main board, Firmware generation environment, control of temperature, and pumps-, Firmware upgrade environment, auto calibration for assays, USB installation Drivers)", Micro2DNA project, 31/07/2007

IR41. L. Bisdounis, S. Blionas, M. Speitel, E. Macii, S. Nikolaidis, A. Milidonis, M. Bonno DS2: Design story II, EASY IST-2000-30093, 2004

IR42. L. Bisdounis, A. Vontzalidis, S. Kougia, L. Tsoura, T. Pagonis, F. Ieromnimon, A. Tatsaki, C. Dre, S. Blionas, P. Delamotte, M. Speitel, O. Abderrahim, D32: System's macrocells – Final, EASY IST-2000-30093, 2004

IR43. L. Bisdounis, S. Blionas, A. Tatsaki, A. Vontzalidis, T. Pagonis, M. Speitel, P. Delamotte, D34: Integration of the overall system, EASY IST-2000-30093, 2004

IR44. C. Dre, L. Bisdounis, D. Metafas, S. Blionas, F. Ieromnimon, A. Tatsaki, Ph. Rouzet, P. Delamotte, E. Macii, M.C. Avalle, M. Speitel, DS1: Design story I , EASY IST-2000-30093, 2003

IR45. L. Bisdounis, S. Blionas, C. Drosos, A. Tatsaki, C. Dre, D35: Low-level hardware-software co-simulation results, EASY IST-2000-30093, 2003

IR46. Bisdounis, T. Trimis, S. Blionas, D41: EASY board - Preliminary report L, EASY IST-2000-30093, 2003

IR47. ASPIS OMI project Synopses, "Telecommunication Specific Processor and Instruction set", S. V. Blionas, Embedded Systems Design, Cornelis Bruin and Frank Cunningham, CHESHIRE HENBURY, 1999, ISBN 1-901864-03-0.

IR48. C. Dre, C. Drosos, S. Blionas, 'ASPIS chip Validation Report', D5.1.IR1, ASPIS, EP20287 (OMI), 1999.

IR49. D. Metafas, M. Zayadin, C. Drosos, S. Blionas, 'Dual mode portable phone demonstrator on an ARM-embedded processor using the Virtuoso Mobile OS', D3.1.D1, ARMOR, EP29251, 1999.

IR50. C. Potamianos, C. Katis, C. Dre, S. Blionas, 'System study and MCM design of the digital part of a mobile phone', D1.1.2, FLINT, EP23261, 1999.

IR51. C. Potamianos, C. Dre, S. Blionas, 'Definition of the technical specifications for the digital part of a mobile phone', D1.1.1, FLINT, EP23261, 1999.

IR52. S. Plevridis, C. Katis, L. Papanastasiou, S. Blionas, 'DC Offset Compensation and AGC Control of a Direct Conversion DECT/GSM Transceiver', INTRACOM Internal Report, 1999.

IR53. G. Kalyvas, D. Soudris, C. Goutis, C. Katis, C. Dre, S. Blionas 'Optimized GSM/DECT Algorithms for the GSM/DCS1800 MODEM', D2.3R1, LPGD, EP25256, 1998.

IR54. G. Kalyvas, C. Katis, C. Dre, S. Blionas, 'Study, Analysis, and Exploration of Candidate Algorithms for a GSM/DCS1800 MODEM', D2.1R1, LPGD, EP25256, 1998.

IR55. C. Dre, C. Katis, S. Blionas, 'Application Requirements of the GSM/DCS1800 MODEM', D3.1R1, LPGD, EP25256, 1998.

IR56. C. Dre, S. Blionas, 'Architectural Description Compatible with the ASPIS Processor, and Simulation Results in the ASPIS Context', D3.5R1, LPGD, EP25256, 1998.

IR57. F. Ieromnimon, C. Dre, D. Moolinar, B. Gyselinx, S. Blionas, 'Report on ASPIS processor Integration', D3.2.R3, ASPIS, EP20287 (OMI), 1998.

IR58. D. Metafas, M. Zayadin, S. Blionas, 'High level model of MAC-layer processes in C and VHDL', D4, EP24129, 1998.

IR59. Δ. Μετάφας, Δ. Μήτσαινας, S. Blionas, 'Σχεδιασμός υποσυστήματος Synchronous Termination Unit και προδιαγραφές Tributary Unit Payload Processor ASIC', Π1.2.1, ΕΠΕΤ ΙΙ 487, 1997.

IR60. Δ. Μετάφας, Δ. Μήτσαινας, S. Blionas, 'Σχεδιασμός υποσυστήματος Framer Deframer Unit και προδιαγραφές Framer/Deframer ASIC', Π1.3.1, ΕΠΕΤ ΙΙ 487, 1997.

IR61. D. Metafas, M. Zayadin, S. Blionas, 'Report on DECT/MAC layer implementation,, D25, CODAC, EP24129, 1997.

IR62. F. Ieromnimon, C. Dre, S. Blionas, 'Report on ARM-peripherals co-simulation in the ASPIS processor', D3.2.R2, ASPIS, EP20287 (OMI), 1997.

IR63. B. Karathanasis, C. Dre, S. Blionas, 'ASPIS Memory mapped blocks, Design Review', D3.1.IR2, ASPIS, EP20287 (OMI), 1997.

IR64. D. Moolinar, B. Gyselinx, C. Dre, F. Ieromnimon, S. Blionas, V. Bella, 'Documentation of the RT-level VHDL code of the multi-mode ASPIS core', D4.2.R2, ASPIS, EP20287 (OMI), 1997.

IR65. C. Dre, H. Karathanasis, D. Moolinar, B. Gyselinx, F. Ieromnimon, S. Blionas, 'ASPIS Processor Core Design Review', D4.2.IR2, EP20287 (OMI), 1997.

IR66. H. Karathanasis, C. Dre, S. Blionas, 'Review of the ASPIS chip design and benchmarking with technology and marketing criteria, D5.1.R2, ASPIS, EP20287 (OMI), 1997.

IR67. Δ. Κριθαρίδης, Δ. Μετάφας, S. Blionas, 'Έλεγχος Physical Interface Low Path Adaptation ASIC', Π1.1.4, ΕΠΕΤ ΙΙ 487, 1996.

IR68. Δ. Κριθαρίδης, Δ. Μετάφας, S. Blionas, 'Λογικός σχεδιασμός Physical Interface Low Path Adaptation ASIC', Π1.1.2.a, ΕΠΕΤ ΙΙ 487, 1996.

IR69. C. Dre, S. Blionas, 'ASPIS, a DECT/GSM Baseband Processor Chip, Benchmarking and Market Positioniong Criteria' D5.1.R1, ASPIS, EP20287 (OMI), 1996.

IR70. H. Karathanasis, C. Dre, S. Blionas, 'ASPIS Building Blocks preliminary design report (memory-mapped)' D3.1.R1, ASPIS, EP20287 (OMI), 1996.

IR71. D. Moolinar, B. Gyselinx, C. Dre, F. Ieromnimon, S. Blionas, 'ASPIS Processor System Architecture (Core + Peripherals)' D2.1.R1, ASPIS, EP20287 (OMI), 1996.

IR72. H. Karathanasis, C. Dre, S. Blionas, 'ASPIS, Final System Level Architecture', D2.3.R1, ASPIS, EP20287 (OMI), 1996.

IR73. Δ. Κριθαρίδης, Δ. Μετάφας, S. Blionas, 'Σχεδιασμός υποσυστήματος Tributary Termination Unit και προδιαγραφές του Physical Interface Low Path Adaptation ASIC' Π1.1.1, ΕΠΕΤ ΙΙ 487, 1995 .

IR74. Δ. Κριθαρίδης, Β. Κασσούρας, Δ. Μετάφας, S. Blionas, 'Προδιαγραφές Ολοκληρωμένων Κυκλωμάτων συστήματος Sub-SDH', Π0.2.2, ΕΠΕΤ ΙΙ 487, 1995.

IR75. Δ. Μετάφας, Δ. Μήτσαινας, Σ. Μπλιώνας 'Λεπτομερές block διάγραμμα συστήματος Sub-SDH' Π0.2.1, ΕΠΕΤ ΙΙ 487, 1995.

IR76. C. Potamianos, J. Hallas, D. Kikidis, S. Blionas, 'Linking a VLSI specific library with an uncommitted library', D1.6.3.4.10, QUICKCHIPS III, EP6043, 1995.

IR77. C. Potamianos, J. Hallas, D. Kikidis, C. Goutis, S. Blionas, 'Enhanced uncommitted VLSI library', D1.6.2.1.5, QUICKCHIPS III, EP6043, 1995.

IR78. N. Κυρλόγλου, S. Blionas, 'Μεθοδολογία σχεδιασμού για πολύπλοκες εφαρμογές' DP1.6, HVLSI-STRIDE 187, 1994.

IR79. C. Potamianos, J. Hallas, D. Kikidis, S. Blionas, 'Computer Aided VLSI Design framework analysis', D1.6.1.1.1, QUICKCHIPS III, EP6043, 1994.

IR80. C. Potamianos, J. Hallas, D. Kikidis, C. Goutis, S. Blionas, 'Independent IC blocks Database', D.1.6.2.2.8, QUICKCHIPS III, EP6043, 1994.

IR81. N. Κυρλόγλου, S. Blionas, 'VLSI Αρχιτεκτονική και λειτουργία επεξεργαστή Viterbi', DP1.3, HVLSI-STRIDE 187, 1994.

IR82. G. Danavaras, D. Dervenis, S. Blionas, 'Prototype Testing results of the Mixed A/D Power meter', D.2.2.3.2, D.6.2.2, HDPE-II EP7503, 1994.

IR83. D. Dervenis, V. Halkiadakis, S. Blionas, 'Report on the Design Service Center environment for mixed analog-digital design', D.2.1.2, HDPE-II, EP7503, 1993.

IR84. D. Dervenis, G. Danavaras, T. Georgantas, S. Blionas, 'A Power meter ASIC: back-annotated simulation results, layout', D.2.2.3.1, HDPE-II EP7503, 1993.

IR85. D. Dervenis, N. Kyrloglou, C. Potamianos, S. Blionas, 'Report on a Digital Testing environment (Hardware infrastructure)', D.6.1.1, HDPE-II EP7503, 1993.

IR86. D. Dervenis, N. Kyrloglou, C. Potamianos, S. Blionas, 'Report on a Digital Testing environment (Software infrastructure)', D.6.1.2, HDPE-II EP7503, 1993.
IR87. C. Potamianos, J. Hallas, D. Kikidis, C. Goutis, S. Blionas, 'Core of an uncommitted VLSI Design library', D1.6.2.1.4, QUICKCHIPS III, EP6043, 1993.
IR88. C. Potamianos, J. Hallas, D. Kikidis, S. Blionas, 'Vendors' VLSI Design libraries and designers' requirements', D1.6.2.2.7, QUICKCHIPS III, EP6043, 1993.
IR89. V. Halkiadakis, J. Tsividis, S. Blionas, 'Infrastructure for Training on ASIC design', D2.1, HVLSI-DPE I, EP5692, 1992.
IR90. D. Lykouropoulos, V. Halkiadakis, S. Blionas, 'Design of a PCM Alarm Unit ASIC D3.1', HVLSI-DPE I, EP5692, 1992.
IR91. V. Halkiadakis, G. Plakas, S. Blionas, 'Establishment of a VLSI Design Environment', D1, HVLSI-DPE I, EP5692, 1991.